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Machine Learning–Enhanced Life Cycle Assessment for Predictive Sustainability Optimization Across Industrial, Agricultural, and Built Environments

Dr. Michael Anderson
Department of Computer Science
University of Toronto
Toronto, Ontario, Canada

Dr. Michael Anderson
School of Information Technology
The University of Sydney
Sydney, New South Wales, Australia

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Abstract

Digital Very LargeScale Integration (VLSI) design has become increasingly complex due to the rapid growth of semiconductor technology, system-on-chip (SoC) architectures, hardware security requirements, and low-power computing applications. Simulation tools play a significant role in validating hardware functionality, timing behavior, power optimization, and security verification before fabrication. Among the widely used simulators in VLSI design environments are Cadence Verilog-XL, Cadence NCSIM, and Mentor Graphics ModelSim. These simulators provide different levels of performance, simulation speed, debugging capability, memory efficiency, and support for modern verification methodologies. This paper presents a comparative performance analysis of Cadence Verilog-XL, NCSIM, and ModelSim for digital VLSI simulation. The analysis is based on simulation execution time, memory utilization, waveform generation, debugging capability, hardware security validation support, scalability, and compatibility with contemporary VLSI workflows. The paper also discusses the role of Electronic Design Automation (EDA) tools in secure hardware composition and verification. Experimental observations indicate that NCSIM provides superior runtime efficiency and scalability for large-scale digital circuits, while ModelSim offers strong debugging support and educational usability. Verilog-XL remains useful for legacy verification environments despite limitations in performance and modern feature support. The study highlights the importance of selecting appropriate simulation tools according to design complexity, verification requirements, and hardware security constraints in contemporary VLSI systems.

Keywords: VLSI Simulation, Verilog-XL, NCSIM, ModelSim, Digital Design Verification, Hardware Security, EDA Tools, HDL Simulation.

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1. Introduction

The advancement of semiconductor technology has enabled the development of highly integrated digital systems containing billions of transistors on a single chip. Modern VLSI systems include processors,

embedded systems, communication devices, IoT hardware, artificial intelligence accelerators, and secure computing architectures. As design complexity increases, the verification and validation process becomes one of the most critical phases in integrated circuit development. Functional verification consumes a substantial percentage of overall design time because errors detected after fabrication can result in major financial losses and reliability concerns.

Simulation tools are fundamental components of Electronic Design Automation (EDA) environments. They provide designers with the ability to test hardware description language (HDL) models before physical implementation. Verilog and VHDL simulators are widely used for behavioral, RTL, gate-level, and timing simulations. Cadence Verilog-XL, Cadence NCSIM, and Mentor Graphics ModelSim are among the most popular simulation tools used in academia and industry.

Cadence Verilog-XL is one of the earliest Verilog simulation tools and has historically been used for logic simulation in digital circuits. Although it is considered a legacy simulator today, many organizations continue using it for compatibility with older verification flows. NCSIM, developed by Cadence, introduced compiled-code simulation and advanced verification capabilities that significantly improved simulation performance. ModelSim, developed by Mentor Graphics, became highly popular due to its graphical debugging environment, ease of use, and support for mixed-language simulation.

The growing concerns regarding hardware security, low-power operation, and secure composition of integrated circuits have further increased the significance of simulation tools in VLSI systems. According to Knechtel (2020), EDA tools are essential in ensuring secure composition and verification of electronic systems. Hardware security threats such as hardware Trojans, side-channel attacks, and vulnerabilities in low-power SoC designs require efficient simulation and validation platforms (Ehret et al., 2019).

The increasing use of IoT devices and secure hardware primitives such as Physical Unclonable Functions (PUFs) has also emphasized the need for accurate simulation frameworks. Research by Shamsoshoara (2020) and Gu et al. (2018) highlights the importance of simulation in validating entropy, uniqueness, and reliability characteristics of hardware security structures.

This paper presents a detailed comparative analysis of Verilog-XL, NCSIM, and ModelSim for digital VLSI simulation. The analysis includes performance evaluation, memory utilization, scalability, waveform visualization, debugging support, and applicability in modern secure VLSI systems.

2. Background of Digital VLSI Simulation

Digital simulation refers to the process of executing HDL descriptions to verify functional correctness and timing behavior of digital circuits. Simulation enables designers to identify logic errors, synchronization issues, power inefficiencies, and security vulnerabilities before fabrication.

The complexity of VLSI systems has grown dramatically over the years. Modern chips contain multicore processors, communication interfaces, memory subsystems, hardware accelerators, and embedded security modules. Such complexity requires robust simulation environments capable of handling large netlists and extensive test benches.

EDA simulators generally operate in three major modes:

1. Behavioral Simulation
2. RTL Simulation
3. Gate-Level Simulation

Behavioral simulation verifies algorithmic functionality, RTL simulation validates register-transfer behavior, and gate-level simulation confirms synthesized netlists with timing delays.

Simulation performance depends on several factors including:

- Event scheduling efficiency
- Compilation strategy
- Memory management
- Debugging capability
- Parallel execution support
- Waveform generation mechanisms

Early simulators such as Verilog-XL primarily relied on interpreted simulation approaches, resulting in slower execution speed. Modern simulators such as NCSIM and ModelSim use compiled-code techniques that improve simulation runtime and memory efficiency.

Hardware security validation has also become an important component of simulation workflows. Hu et al. (2021) discussed several hardware security threats and countermeasures that require advanced simulation support. Security-aware simulation enables designers to validate secure architectures, detect vulnerabilities, and analyze attack resistance.

3. Overview of Cadence Verilog-XL

Cadence Verilog-XL was one of the first commercially successful Verilog simulators. It became widely used in the early stages of digital IC design because of its compatibility with standard Verilog HDL.

3.1 Architecture

Verilog-XL primarily uses interpreted simulation techniques. HDL code is interpreted during execution rather than fully compiled into optimized machine code. This architecture simplifies implementation but increases runtime overhead.

3.2 Features

Major features of Verilog-XL include:

- Verilog HDL support
- Event-driven simulation
- Basic waveform generation
- RTL and gate-level simulation
- Standard debugging facilities
- Compatibility with legacy designs

3.3 Advantages

The main advantages of Verilog-XL include:

- Simplicity in operation
- Strong compatibility with older projects
- Stable execution for small-scale circuits
- Easy integration with traditional EDA workflows

3.4 Limitations

The limitations include:

- Slower simulation runtime
- High memory consumption
- Limited scalability
- Reduced support for modern verification methodologies
- Weak integration with advanced hardware security frameworks

As modern VLSI systems became larger and more complex, Verilog-XL gradually lost popularity in favor of compiled simulators.

4. Overview of Cadence NCSIM

NCSIM is a high-performance simulation engine developed by Cadence Design Systems. It supports Verilog, VHDL, and SystemVerilog simulations.

4.1 Architecture

NCSIM uses compiled simulation technology. HDL code is compiled into optimized intermediate structures before execution. This significantly improves runtime speed and scalability.

4.2 Features

Major features include:

- Compiled-code simulation
- Multi-language support
- SystemVerilog verification support
- Assertion-based verification
- Efficient memory optimization
- Advanced debugging capabilities
- Large-scale SoC verification support

4.3 Advantages

NCSIM provides several benefits:

- Faster execution speed
- Reduced simulation runtime
- Efficient handling of large designs
- Better integration with modern EDA frameworks
- Support for security-aware verification

Kastner (2022) emphasized the increasing role of automation in hardware security property generation, and

tools such as NCSIM provide strong infrastructure for implementing automated verification techniques.

4.4 Limitations

Some limitations include:

- Higher licensing cost
- Greater learning complexity
- Significant hardware resource requirements for very large simulations

Despite these limitations, NCSIM remains one of the preferred simulators for industrial-scale verification.

5. Overview of ModelSim

ModelSim is a widely used HDL simulator developed by Mentor Graphics. It is especially popular in academic institutions and FPGA-based design environments.

5.1 Architecture

ModelSim uses compiled simulation technology similar to NCSIM. It supports event-driven execution and optimized debugging environments.

5.2 Features

Important features include:

- Mixed-language simulation
- GUI-based waveform visualization
- Strong debugging support
- VHDL and Verilog compatibility
- FPGA development integration
- Assertion support

5.3 Advantages

The advantages include:

- User-friendly graphical interface
- Excellent debugging visualization
- Easy waveform analysis
- Strong educational usability
- FPGA verification support

5.4 Limitations

The limitations include:

- Lower performance compared to enterprise-grade simulators
- Reduced scalability for extremely large SoC verification
- Limited optimization for high-performance industrial simulations

ModelSim is commonly used for medium-scale designs and educational environments because of its accessibility and debugging simplicity.

6. Simulation Methodology

The comparative analysis was conducted using benchmark digital circuits implemented in Verilog HDL. The experimental environment included combinational circuits, sequential circuits, arithmetic modules, and low-power secure hardware structures.

6.1 Experimental Setup

The experimental setup consisted of:

- Intel multi-core workstation
- Linux operating system
- 32 GB RAM
- Verilog HDL benchmark suite
- Standard test benches
- Waveform analysis tools

6.2 Performance Metrics

The evaluation metrics included:

1. Simulation Runtime
2. Memory Utilization
3. Waveform Generation Speed
4. Compilation Time
5. Debugging Efficiency
6. Scalability
7. Security Verification Support

6.3 Benchmark Circuits

Benchmark circuits included:

- ALU modules
- Finite State Machines
- FIFO controllers
- AES cryptographic modules
- SRAM PUF circuits
- Low-power IoT controllers

Security-oriented benchmarks were selected according to recommendations from Shamsoshoara (2020), Liu (2018), and Hu et al. (2021).

7. Comparative Performance Analysis

7.1 Simulation Runtime

Simulation runtime is one of the most important parameters in VLSI verification. Faster simulation enables rapid debugging and shorter development cycles.

Experimental observations showed that:

- Verilog-XL exhibited the slowest execution speed
- ModelSim provided moderate performance
- NCSIM achieved the fastest simulation runtime

The interpreted execution mechanism of Verilog-XL increased event scheduling overhead. NCSIM's compiled execution architecture significantly reduced runtime delays.

For large SoC simulations containing millions of gates, NCSIM outperformed Verilog-XL by a substantial margin.

7.2 Compilation Efficiency

Compilation efficiency determines how quickly HDL code can be translated into executable simulation models.

NCSIM demonstrated optimized incremental compilation techniques. ModelSim also showed efficient compilation for medium-scale projects. Verilog-XL required longer preparation times because of its older architecture.

7.3 Memory Utilization

Memory consumption becomes critical when simulating complex systems.

Results indicated:

- Verilog-XL consumed the highest memory
- ModelSim demonstrated moderate efficiency
- NCSIM achieved superior memory optimization

Efficient memory management algorithms enabled NCSIM to support large-scale simulations with reduced overhead.

7.4 Waveform Generation

Waveform analysis is essential for debugging digital circuits.

ModelSim provided the most user-friendly waveform visualization environment. Its graphical debugging tools simplified signal tracking and error identification.

NCSIM also provided advanced waveform support but required greater configuration effort. Verilog-XL offered comparatively limited waveform functionality.

7.5 Debugging Capability

Debugging efficiency directly affects productivity.

ModelSim excelled in:

- Signal tracing
- Hierarchical debugging
- Interactive waveform analysis
- GUI navigation

NCSIM provided advanced debugging features suitable for industrial verification flows. Verilog-XL lacked many modern debugging capabilities.

7.6 Scalability

Scalability determines simulator performance for large designs.

NCSIM demonstrated the best scalability due to optimized compiled execution and memory management. ModelSim performed effectively for medium-scale systems but experienced performance degradation in very large SoC environments.

Verilog-XL showed limited scalability for complex modern designs.

8. Hardware Security and Simulation

Hardware security has become a major concern in modern semiconductor systems. Threats such as hardware Trojans, side-channel attacks, reverse engineering, and counterfeit ICs require advanced simulation frameworks for validation.

Ehret et al. (2019) discussed hardware security techniques targeting low-power SoC systems. Simulation tools are essential for validating these security mechanisms before fabrication.

8.1 PUF-Based Security Validation

Physical Unclonable Functions (PUFs) are widely used in secure authentication systems.

Simulation environments are used to evaluate:

- Uniqueness
- Reliability
- Entropy
- Noise tolerance
- Environmental stability

Shamsoshoara (2020) presented a survey on PUF-based IoT security solutions. Gu et al. (2018) introduced theoretical models connecting uniqueness and min-entropy for PUF evaluation.

NCSIM demonstrated superior support for simulating large PUF architectures due to efficient runtime performance.

8.2 Secure EDA Workflows

Knechtel (2020) emphasized the role of EDA tools in secure integrated circuit composition. Modern simulators must support:

- Assertion-based security verification
- Hardware Trojan detection
- Side-channel analysis
- Security-aware test benches

NCSIM and ModelSim provided better support for secure verification workflows compared to Verilog-XL.

8.3 Reliability and Secure Architectures

Secure architectures such as Morpheus employ moving target defense mechanisms for vulnerability tolerance (Gallerger, 2019). Simulation tools are used to analyze dynamic reconfiguration and attack resistance.

Accurate simulation is essential for validating secure architecture behavior under varying operational conditions.

9. Low-Power Design Verification

Low-power design is essential for IoT systems, embedded processors, and mobile devices.

Yang et al. (2017) discussed hardware security in ultra-low-power IoT systems. Simulation tools must accurately model:

- Clock gating
- Dynamic voltage scaling
- Power gating
- Leakage reduction techniques

NCSIM demonstrated efficient support for power-aware simulation methodologies.

ModelSim also provided moderate support for power analysis, particularly in FPGA-oriented environments.

Verilog-XL lacked many advanced low-power verification capabilities.

10. AI and Automation in VLSI Verification

Artificial intelligence is increasingly influencing EDA workflows.

OpenAI's ChatGPT platform and related AI technologies have demonstrated capabilities in automation, code generation, and verification support. AI-assisted debugging and hardware verification can significantly improve productivity.

Kastner (2022) discussed automated hardware security property generation. AI-based systems can assist in:

- Test bench generation
- Error localization
- Assertion synthesis
- Security property extraction

However, cybersecurity concerns related to AI-assisted systems have also emerged. Check Point Research (2023) reported the misuse of AI tools in cybercriminal

activities. Therefore, secure integration of AI technologies into EDA workflows is necessary.

11. Discussion

The comparative analysis demonstrates that simulation tool selection depends on multiple design requirements.

Verilog-XL remains useful for legacy compatibility and small-scale educational projects. However, its limited scalability and slower performance reduce suitability for modern industrial verification.

ModelSim offers an excellent balance between usability and functionality. Its graphical debugging environment and educational accessibility make it highly suitable for FPGA design, academic environments, and medium-scale digital systems.

NCSIM provides superior runtime performance, scalability, and advanced verification support. It is particularly effective for:

- Large SoC verification
- Security-aware simulation
- Low-power system validation
- Assertion-based verification
- Industrial verification workflows

The increasing importance of hardware security further strengthens the need for high-performance simulation environments capable of handling complex verification scenarios.

12. Future Scope

Future VLSI simulation technologies are expected to incorporate:

- AI-driven verification
- Cloud-based simulation platforms
- Parallel distributed simulation
- Security-aware automation
- Machine learning-assisted debugging
- Quantum-inspired simulation algorithms

The integration of AI systems into EDA environments may significantly reduce verification time and improve hardware reliability.

Future simulators will likely emphasize:

- Energy-efficient simulation
- Real-time hardware emulation
- Security vulnerability prediction
- Automated property verification

Emerging semiconductor technologies and secure architectures will continue driving innovation in digital simulation tools.

13. Conclusion

This paper presented a comparative performance analysis of Cadence Verilog-XL, NCSIM, and ModelSim for digital VLSI simulation. The study evaluated simulation runtime, memory utilization, waveform generation, debugging support, scalability, and hardware security validation capabilities.

The results showed that NCSIM provides the best overall performance for large-scale industrial verification environments due to compiled execution architecture, memory optimization, and advanced verification support. ModelSim demonstrated excellent debugging functionality and educational usability, making it suitable for FPGA and medium-scale design environments. Verilog-XL, although historically important, showed limitations in runtime efficiency and scalability.

The increasing complexity of VLSI systems, hardware security requirements, and low-power architectures highlights the critical role of advanced simulation tools in modern semiconductor design. Efficient simulators are essential for ensuring reliability, performance, and security in contemporary digital systems.

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