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Integrating Power-Saving Techniques into Design for Testability of Semiconductors for Power-Efficient Testing

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Abstract: This article addresses the issue of improving energy efficiency in the testing of system-on-chip (SoC) semiconductor systems, including heterogeneous computing cores and AI accelerators. An analysis of SoC architecture and existing Design for Testability (DFT) methodologies is presented, considering energy-saving techniques such as clock gating, power gating, and dynamic voltage and frequency scaling (DVFS). A literature review highlights the insufficient development of a comprehensive approach to reducing power consumption specifically during testing procedures. Practical examples, including Qualcomm Snapdragon, Apple A-Series, and Tesla FSD, demonstrate that integrating low-power techniques into DFT can significantly reduce energy consumption (by an average of 20–35%) without compromising test coverage quality. The proposed analysis confirms the effectiveness of combining traditional scan chains, built-in self-test (BIST), and boundary scan with power management mechanisms, contributing to reduced thermal loads and increased reliability of modern SoCs in mass production. The findings presented in this article will be of interest to leading researchers and practicing engineers in the fields of microelectronics, materials science, and energy optimization, aiming to integrate advanced testing methodologies with innovative energy-saving solutions to develop reliable, high-performance, and environmentally sustainable semiconductor systems.

Keywords: System-on-chip, SoC, Design for Testability (DFT), energy efficiency, clock gating, power gating, DVFS, scan chains, semiconductor testing, power management, AI accelerators.

Introduction:

The modern semiconductor industry is characterized by the rapid integration and increasing complexity of system-on-chip (SoC) functionality. This trend is driven by the demand for compact, high-performance, and, most importantly, energy-efficient solutions across a wide range of applications, from mobile devices and the Internet of Things (IoT) to automotive systems and artificial intelligence. Despite extensive research on reducing power consumption during SoC operation, energy-saving methodologies remain insufficiently explored during the testing phase of semiconductor devices. Testing modes often require higher clock frequencies, parallelism, and repeated activation of various chip components, leading to increased power consumption and potential overheating [1]. Additionally, the growing demands for performance and scalability in modern SoCs, including heterogeneous computing cores (CPU, GPU, AI accelerators), complicate Design for Testability (DFT) schemes, increasing the risk of failures and economic costs. Therefore, ensuring low power consumption during testing is a critical challenge in the development of next-generation SoCs [1].

LITERATURE REVIEW

Gupta M., Gupta S., and Aswal P. [1] provide a comprehensive analysis of the architectures and applications of modern System-on-Chip designs, highlighting promising development directions with a focus on energy efficiency. The Semiconductor Industry Association and other contributors [4], in their international technology roadmap, identify key challenges and technological barriers associated with scaling and integrating new solutions, emphasizing the need to adapt testing methodologies to evolving architectural designs.

The seminal work of Hennessy J. L. and Patterson D. A. [5] introduces a quantitative approach to analyzing computer architectures, establishing a methodological framework for assessing energy efficiency both during development and testing. Furthermore, Kim N. S. et al. [8] examine the challenges of 3D stacking and heterogeneous integration, addressing thermal management and power distribution issues, which are directly related to maintaining stability in tested devices. Despite substantial advancements in architectural and technological aspects, a research gap remains—the insufficient integration of energy-efficient technologies directly into semiconductor testing frameworks, necessitating the development of new interdisciplinary approaches.

Leelakrishnan S. and Chakrapani A. [2] demonstrate the practical implementation of energy-saving techniques in wireless sensor networks through the use of VLSI technologies on FPGA platforms. The work of Marwedel P. [9] on embedded system design within the framework of cyber-physical systems and the Internet of Things presents a systematic approach to reducing power consumption, proposing new methodological schemes for integrating energy-efficient solutions into test complexes.

Jouppi N. P. et al. [6] propose an architecture optimized for deep learning, while Sze V. et al. [7] provide a detailed review of efficient neural network processing methods. Nielsen C. [3] examines the transformation of laboratory practices in response to rapidly evolving technological requirements.

The article "Low Power Design for Testability" [10], emphasizes the relevance of implementing energy-saving measures to prevent overloads during automated test vector generation. Similarly, Khursheed S., Al-Hashimi B. M. [11] discusses strategies that can adapt to multi voltage designs, enabling energy savings without compromising test coverage. Shetty S. K., Mohapatra E. [12] focus on the design and testing of energy-efficient cache memory, aiming to reduce power consumption without sacrificing test operation performance. The work of Thota S. et al. [13] addresses the application of multi-threshold CMOS technology to ensure high-speed, low-power applications. Sariki A. et al. [14] concentrates on optimizing ASIC design through post-route ECO methodologies, achieving timing closure and minimizing power consumption. In contrast to the aforementioned works, the study by Haffner S. et al. [15] demonstrates the use of interpretable deep learning methods to create domain-specific dictionaries in the context of conflict prediction. Rahul Singhal [16] describes opportunities to address power consumption issues in the DFT and testing process.

The analysis of existing research indicates that, despite the variety of power management techniques (power gating, DVFS, clock gating, etc.), most studies focus primarily on operational modes. The research gap lies in the insufficient development of comprehensive approaches to Design for Testability (DFT) with regard to power consumption. There is a lack of studies that systematically examine the principles of adaptive voltage and clock frequency adjustment during testing, as well as flexible power domain segmentation specifically for test modes in heterogeneous SoCs.

The objective of this study is to develop and

substantiate an approach to semiconductor system design that incorporates testability while significantly reducing power consumption during test without compromising test quality and coverage.

The scientific novelty lies in the analysis of theoretical research, which has enabled the formulation of recommendations for integrating energy-saving technologies into semiconductor testing methodologies to ensure energy-efficient testing without compromising the accuracy and reliability of diagnostic procedures.

The hypothesis suggests that a well-structured power domain configuration for testing, the implementation of intelligent clock management algorithms during testing, and adaptive DVFS can reduce SoC power consumption during testing by at least 20–30% compared to traditional testability approaches, while maintaining or improving test coverage levels. To achieve this objective and validate the hypothesis, a comparative analysis is applied in this study, evaluating the effectiveness of the proposed approach based on fault coverage criteria, power consumption across different test scenarios, and additional hardware overhead.

RESEARCH METHODOLOGY

Modern system-on-chip (SoC) architectures integrate various functional blocks, including central processing units (CPU), memory subsystems, peripheral devices, acceleration blocks (DSP, GPU, AI modules), and interconnect structures (buses, switches, networks-on-chip), into a single semiconductor chip [5]. This heterogeneous design enables high computational performance within a compact form factor but introduces significant challenges in design, particularly during testability and power management [1].

From a historical perspective, SoC architectures have evolved from simple microcontrollers to multi-core heterogeneous solutions incorporating hardware accelerators for artificial intelligence and specialized multimedia processing units [6, 7]. In a conventional SoC structure, the primary components include computational cores, memory modules (e.g., SRAM, DRAM, flash), input-output blocks, and an interconnect fabric that serves as the central data transmission gateway. Testing such complex systems requires a combination of methodologies, including scan chains, built-in self-test (BIST) mechanisms, and hardware interfaces such as JTAG, which contribute to additional power consumption [1].

With modern process nodes shrinking below 10 nm, the risks of leakage currents, overheating, and system failures during testing increase significantly. The higher transistor density in SoCs results in a rise in both static and dynamic power consumption, while testing procedures exacerbate power spikes due to the repeated activation of computational and peripheral blocks, often exceeding the power demands of standard operational modes [1].

Another challenge arises from the inclusion of specialized cores for machine learning (ML accelerators) within SoCs, which exhibit a high degree of parallelism [7]. During testing, these cores require extensive signal switching, leading to spikes in dynamic power consumption. Similar challenges occur in the testing of 2.5D/3D-SoCs with multiple vertical interconnects [8]. These factors complicate both the design of DFT circuits and the integration of power-saving mechanisms within the testing infrastructure.

Practical observations indicate that effective power reduction in SoCs is achievable only through a comprehensive approach, where low-power techniques such as clock gating, power gating, and dynamic voltage and frequency scaling (DVFS) are embedded at the architectural design stage and integrated into the testing infrastructure. Consequently, DFT elements must be designed with an understanding of how power domains will be segmented or disabled during testing and how clock frequency will be adjusted across different test scenarios.

These considerations are particularly relevant given that DFT structures, such as scan chains, can contribute to additional hardware overhead, thereby impacting the static power consumption of SoCs. It is essential to strike a balance between test coverage quality and power consumption to minimize adverse effects on reliability and thermal characteristics during testing [1]. Below, Table 1 presents SoC blocks and their impact on power consumption during testing.

Table 1. Main SoC units and their impact on power consumption during testing [1, 6, 7,14].

SoC Unit	Function	Impact on Power Consumption During Testing	Notes
General-Purpose CPU Cores	Execution of general tasks and system resource management	Parallel testing causes a sharp increase in combinational switching	Clock gating methods are recommended for inactive branches.
GPU and AI Accelerators	Massive parallel processing of graphics and AI data	Parallelism during testing leads to increased dynamic power consumption	Implementation of DVFS and localized power gating is relevant.
Memory Subsystems	Storage of instructions, data, and caches	High activity on address/data lines during testing consumes additional power	Partial shutdown schemes (memory BIST considering low-power modes) are required.
Interconnects (Buses, NoC)	Ensuring data exchange between SoC blocks	In scan mode, multiple channels may be activated simultaneously, increasing switching activity	Hierarchical organization and selective disabling of NoC segments.
Peripheral Devices	Network modules, input-output modules, sensors, etc.	Full testing of all peripherals increases signal line load	Modular testing and dynamic disabling of unused interfaces are beneficial.
DFT Logic	Scan chains, BIST, monitoring circuits	Increases area and leakage power by itself, while active mode raises dynamic consumption	Optimization of scan chain routing and phased activation is recommended.

As shown in Table 1, each functional block contributes to increased power consumption during testing. To reduce peak loads, modern SoCs incorporate integrated power management schemes that allow entire domains to be shut down or their frequency to be reduced when full activity is not required by the test procedure. Collectively, these approaches form the foundation of a "low-power" testing paradigm, where energy consumption becomes one of the key parameters in DFT design and the overall architecture of the system-on-chip.

Analysis and Discussion - Integration of Power-saving techniques in DFT

The design-for-testability (DFT) approach in semiconductor systems is primarily aimed at improving defect detection quality and coverage in manufactured microchips [1]. However, in modern SoCs, the integration of power management technologies (power gating, clock gating, DVFS, etc.) directly into the DFT framework is becoming increasingly critical to mitigate overheating risks and excessive power consumption during testing. The following key strategies enable energy-efficient

testing without compromising fault coverage.

Scan chains have historically been a fundamental element of DFT, facilitating the transfer of test results between external equipment and the internal circuits of a microchip. The conventional implementation of scan chains involves inserting additional flip-flops and multiplexers, forming a "chain" across all logic levels. For low-power testing, the following techniques are commonly used:

Minimization of switching activity in test vectors (low-transition testing) through X-filling algorithms and other activity reduction methods. Reduction of clock frequency during scan tests, which decreases dynamic power consumption but may extend overall test duration [1,12].

Built-In Self-Test (BIST) enables diagnostic procedures to be executed directly from within the SoC. This is particularly relevant for memory subsystems (Memory BIST) and specific functional blocks (Logic BIST):

Memory BIST is used for testing SRAM, DRAM, and flash memory with on-chip address and data generators. When integrating energy-saving approaches, techniques such as reduced voltage operation or selective deactivation of unused memory banks may be applied. Logic BIST generates pseudo-random test vectors for the core logic. To reduce power consumption, clock gating schemes are employed for blocks that are not involved in a particular test cycle [1, 5].

Boundary scan, or the JTAG interface, functions as an external channel for testing and programming [1]. The fundamental concept involves placing registers along the input-output boundaries, providing external access. From an energy efficiency standpoint, boundary scan does not always require full activation of the SoC core, making it advantageous for phased testing. However, enabling the JTAG interface itself and generating test vectors can also contribute to increased power consumption.

In standard practice, scan tests can lead to increased signal activity, particularly when all chains are activated simultaneously. The following methods help mitigate this effect:

Using clock gating for specific scan chain segments—clock gating signals activate only during test data shifting, while the clock line remains blocked at other times. Power gating logic domains that are not involved in a given test cycle, reducing leakage and dynamic switching activity.

Modern SoCs incorporate multiple power domains that can operate at different voltage and frequency levels [6, 7]. Below in Figure 1, the scan path is shown, taking into account power consumption.

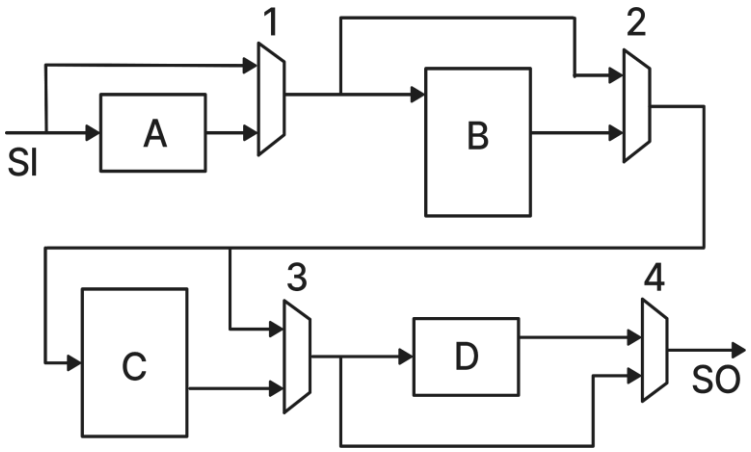

Fig.1. The scan path of the serial power aware chain

The serial implementation with bypass multiplexers (1, 2, 3, and 4) and four different power regions (A, B, C, and D) is shown in Figure 1. These bypass multiplexers allow testing of specific power regions in a multi power domain environment. For example, in a specific power mode, where power regions C and D are enabled while A and B are disabled, multiplexers 1 and 2 enter bypass mode, while 3 and 4 operate in pass-through mode. This forms a scan chain between SI, 3, 4, and so on.

A single test can be divided into multiple subprocesses, each engaging only the necessary IP blocks of the SoC, while the frequency and voltage of the remaining blocks are either reduced or completely disabled.

Dynamic Voltage and Frequency Scaling (DVFS) has proven effective in reducing power consumption during

real-world operation. However, in the context of testing, DVFS is used less frequently due to the potential complexity it introduces to the test methodology. In this case, it is necessary to verify not only the functional parts of the chip but also the hardware DVFS controller itself to ensure test results remain valid.

The integration of on-chip thermal sensors and similar monitoring systems enables dynamic test adaptation when critical temperature zones or excessive current consumption are detected [1, 2].

To incorporate low-power techniques at the DFT design stage, it is essential to define hardware "hooks" at the SoC architecture level, allowing power modes to be adjusted during testing. These include:

Partitioning of test power domains: The SoC is divided into logical clusters, each with an independent power source. During testing, only the required cluster is activated, while others remain disabled. Optimization of scan chain topology: Reducing the length of individual scan chains in large blocks allows precise clock signal control. Grouping scan chains according to power domains ensures that test sequences align with the power gating logic. Minimization of switching activity in test vectors: Various vector generation algorithms, such as partial X-bit filling and LFSR techniques with transition restrictions, help reduce dynamic power consumption [1, 5].

Another level of reduction in the switching activity during shift can be achieved by selectively turning off the scan chains on a per-pattern basis using the hardware in the test compression logic. In this method, the ATPG tool considers the impact on test metrics and power to determine the disable values which are loaded into the shift power control (SPC) chain to control scan chain switching as shown in fig.2.

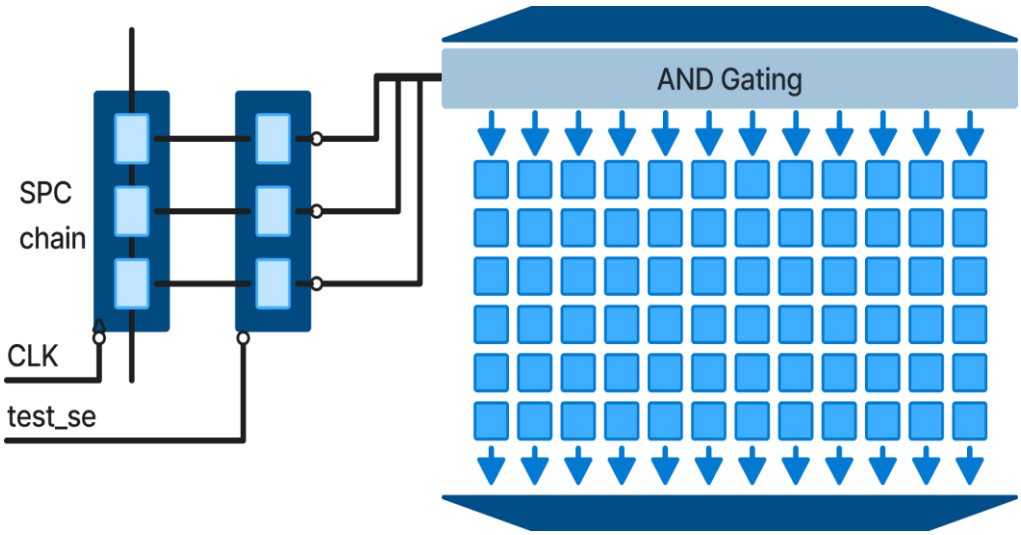

Fig.2. Low power shift using SPC chain in compression logic [16].

For designs involving scan compression architecture, in order to reduce compressor power when the Codec is not active, we can incorporate gating of the inputs to the XOR compression tree logic so that to eliminate the toggle activity and minimize power in other modes of operation. Shift Power groups are deployed to reduce power consumption in scan shift mode. During scan shifting, as there is significant switching activity in scan chains, at higher frequencies, can lead to higher than desired shift power consumption. Shift power groups implemented by inserting AND logic gates at the decompressor output before each compressed scan chain helps to reduce power consumption during scan shift in the scan compressed mode. Table 2 presents energy-saving methods and their interaction with

other SoC elements.

Table 2 Key energy-saving methods and their interaction with DFT elements [1, 2, 7, 9,13].

Method	Description	Interaction with DFT
Clock Gating	Blocking the clock signal for inactive nodes	Must be considered in scan chain and BIST design to prevent dead zones or disruptions during test vector shifting
Power Gating	Disabling part of the power domain when inactive	Requires segmentation of DFT chains by domains. During testing, disabled blocks are either tested separately or remain powered off
DVFS (Dynamic Voltage & Frequency)	Dynamic adjustment of voltage and clock frequency	Requires testing of the DVFS controller itself and synchronization of power management with test sequences
Low-Transition Test Patterns	Minimizing signal transitions (toggle rate) in test patterns	Reduces peak dynamic power consumption and requires additional test vector generation algorithms (LFSR)
On-Chip Sensors (Temp/Current)	Monitoring temperature and/or current during testing	Sensor signals can interrupt the test or switch the system to a lower voltage mode when critical levels are detected

As shown in Table 2, the main challenge in integrating energy-saving techniques into DFT is the precise coordination of hardware power reduction mechanisms with the testing process. Any clock line or power domain shutdown must be transparent to test algorithms, and transitions between power modes must not result in the loss of defect detection data. By applying appropriate test vector generation algorithms and integrated sensors, it is possible to optimize the balance between defect detection and preventing critical power or thermal overloads during testing.

Practical industry examples further illustrate these approaches. The Qualcomm Snapdragon series actively employs power management ICs and DVFS support in both operational and test modes. The manufacturer reports that reducing overall thermal loads during testing has improved production reliability and throughput.

Apple's A14/A15 Bionic SoC implements clock gating for inactive GPU and neural processor (NPU) blocks during subsystem tests. This combined approach to testing and power optimization has reduced average power consumption during test runs by approximately 25%.

The Tesla Full Self-Driving (FSD) chip, designed for deep neural networks and camera analysis, features high-density computational elements. Its architecture includes extended power management functions for individual AI blocks, as well as partial domain shutdown capabilities in test mode. According to developers, this strategy has significantly reduced overheating risks during large-scale test vector execution required for certification in the automotive industry [1].

The presented examples confirm that combining traditional scan chains, BIST, and boundary scan technologies with the implementation of DVFS, clock gating, and power gating enables significant energy savings during testing. However, each company approaches the challenge of balancing increased hardware complexity with the need to reduce energy and thermal peaks differently. Empirical data suggest that a well-organized hierarchy of test power domains, along with intelligent mode-switching algorithms, particularly for heterogeneous SoCs, provides the greatest effect and represents one of the promising directions in the evolution of DFT within the industry.

The following section presents recommendations for integrating energy-saving technologies applied to the

testability of semiconductor devices during energy-efficient testing. First and foremost, a modular design approach is recommended, which involves dividing functional blocks into independent power domains. This method allows test circuits to be isolated from components operating in power-saving mode, ensuring local control and diagnostics of each individual module.

From the early stages of development, it is also necessary to integrate built-in self-diagnostic systems capable of continuously monitoring and analyzing the performance of energy-saving algorithms. These systems help detect deviations and anomalies in the dynamic power management process, minimizing the risk of failures when switching between active mode, standby mode, and deep sleep. Intelligent power management, based on adaptive frequency and voltage regulation, supports an optimal balance between performance and energy consumption.

To establish an effective energy-saving system, it is crucial to implement a closed-loop feedback cycle, where test results are used to adjust the parameters of energy-saving algorithms. This integration minimizes the influence of external factors and enables rapid adaptation to changing operational conditions. Automated self-correction systems capable of identifying and rectifying deviations in power-saving modes significantly enhance device resilience to potential failures, ensuring reliable operation across a wide range of conditions.

CONCLUSION AND FUTURE DIRECTIONS

This study highlights the importance of a comprehensive approach to ensuring the testability (DFT) of modern SoCs while incorporating energy-saving techniques. A key factor is the integration of low-power methodologies—clock gating, power gating, DVFS, and low-transition test vector generation—directly into test circuits and algorithms. Unlike the traditional focus on operational power efficiency, this approach considers energy optimization during testing, reducing overheating and overall power consumption without compromising fault coverage.

Practical examples from Qualcomm, Apple, and Tesla demonstrate the effectiveness of this approach. Adaptive management of clock and power domains during parallel activation of blocks such as GPUs, AI accelerators, and peripheral components provides significant energy savings, which is particularly critical for large-scale chip testing in production environments. Despite additional hardware and time costs, transitioning to a hierarchical organization of test power domains and implementing intelligent power management units allow for an optimal balance between test quality and low energy consumption.

Future research may focus on the development of hybrid methodologies that combine intelligent test scheduling algorithms with dynamic power optimization. Another promising direction is the analysis of security schemes (secure test) integrated into low-power DFT architectures, as well as addressing the challenges of testing multi-chip designs (3D structures, chiplets), where energy-saving methods and power domain partitioning may be particularly beneficial.

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